

**REMARKS**

At the outset, Applicant thanks the Examiner for the thorough review and consideration of the subject application. The Office Action of January 4, 2005 has been received and its contents carefully reviewed.

Claims 7-10 are hereby added. Accordingly, claims 1-10 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

Applicant appreciates the indication of allowable subject matter in claims 4 and 5.

In the Office Action, the Examiner rejected claims 1, 2, and 6 under 35 U.S.C. §103(a) as being unpatentable over Schiefer et al. (U.S. Patent No. 6,177,922). This rejection is respectfully traversed and reconsideration is requested.

Rejecting claim 1, the Examiner cites Figures 1-4 of Schiefer et al. as disclosing “an interface (130...) receiving a timing data ... and a control signal corresponding to the display standard [of a flat panel display device (140)]; a timing controller (330) for latching and outputting the timing data inputted from the interface [130]... , wherein said timing controller includes a decoder (120, fig. 1) and a timing generator (430, fig. 4), wherein timing generation information corresponding to a plurality of display standards is stored by the decoder [120] (see... col. 5., lines 53-55...), wherein the decoder (120) may output to the timing generator [430], timing information corresponding to the timing data, and wherein the timing generator [430] outputs timing signals corresponding to the timing information and the control signal (see column 11, lines 46-60).” Applicant respectfully disagrees.

Specifically, Schiefer et al. teaches wherein the timing controller 330 is included within the format converter 110 (see column 9, lines 12-14). As shown in Figures 1 and 3 of Schiefer et al., the timing controller 330 receives FSYNC, IPCLK, IPCLKEN, IPVSYNC, and IPHSYNC signals output by an input selector 100 but does not receive any of the CLK2, IPCLKEN2, HSYNC2, VSYNC2, or DATA2 signals output by the interface 130. Therefore, Applicant respectfully submits the timing controller 330 of Schiefer et al. does not latch and output timing data inputted from the interface 130, as asserted by the Examiner.

Moreover, and as shown in Figure 1 of Schiefer et al., the decoder 120 is connected between the interface 130 and an input selector 100. Therefore, Applicant respectfully submits that the timing controller 330 of Schiefer et al., which is included within the format converter 110, does not include the decoder 120, as asserted by the Examiner.

Further, at column 5, lines 50-55, Schiefer et al. states “in the case of a digitized and decoded NTSC input source signal the incoming fields of NTSC data can be processed into a progressive scan format and used to drive VGA timing compatible displays, SVGA timing compatible displays, or XGA timing compatible displays.” Further, Applicant respectfully submits that Schiefer et al. is silent as to any teaching or suggestion that the decoder 120 stores “timing generation information corresponding to a plurality of display standards,” as asserted by the Examiner. Accordingly, Applicant respectfully submits that Schiefer et al. fails to teach at least this feature of claim 1.

Still further, Schiefer et al. teaches wherein the timing generator 430 is included within the timing controller 330 (see column 11, lines 44-61). As shown in Figures 1 and 4 of Schiefer et al., the timing generator 430 receives DHLOCKEVENT, DVLOCKEVENT, DTGRUN, and DCLK signals variously output by a display synchronizer 410 and a display clock generator 420 (both included within the timing controller 330) but does not receive any of the CLK1, IPCLKEN1, HSYNC1, VSYNC1, or DATA1 signals output by the decoder 120. Therefore, Applicant respectfully submits the decoder 120 of Schiefer et al. does not output, to the timing generator 430, timing information corresponding to the timing data, as asserted by the Examiner.

For at least the reasons set forth above, Applicant respectfully submits that Schiefer et al. fails to teach or suggest each and every element as recited in claim 1. (see M.P.E.P. § 2143.03) and request withdrawal of the present rejection under 35 U.S.C. § 103(a).

In the Office Action, the Examiner rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over Schiefer et al. in view of Barshinger (U.S. Patent No. 5,049,864). This rejection is respectfully traversed and reconsideration is requested.

Claim 3 depends from claim 1 and, therefore, includes all of the elements recited in claim 1. As discussed above, a Schiefer et al. fails to teach or suggest each and every element

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recited in claim 1. Barshinger fails to cure the deficiency of Schiefer et al. with respect to claim 1. Therefore, Applicants respectfully submit that a *prima facie* case of obviousness has not been established with respect to claim 3. For at least this reason, Applicants respectfully request withdrawal of the present rejection of claim 3 under 35 U.S.C. § 103(a).

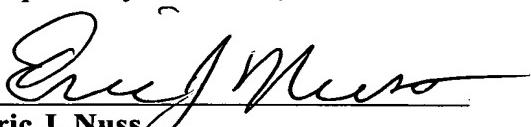
Applicant believes the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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